CLAIMS

1. A method of operating a cache in a computer system, the cache storing items associated with addresses in memory in the computer system, the cache having at least one way with a tag array and a data array, with information in the tag array indicating, for each address applied to the cache, whether information in the data array is associated with the applied address in memory, with the data array implemented as an array of cells connected to lines and a plurality of sense amps, with a sense amp being connectable to each of the lines, comprising, for each of the at least one way:

a) making a determination, based on information stored in the tag array, whether an item associated with the applied address is stored in the way in the data array;

b) altering the state of at least one line in the way associated with the applied address starting before completing the determination ;

c) after completing the determination, when the information indicates an item is stored in the way in the data array, enabling at least one sense amp associated with a line in the way when it is determined that an item associated with the applied address is stored in the way.

2. The method of claim 1 wherein each sense amp is connectable to a plurality of lines and enabling the sense amp associated with a line in the indicated way comprises connecting the sense amp to a single one of the plurality of lines selectively in response to the information read from the tag array.

3. The method of claim 1 additionally comprising providing as a bit in the output of the cache, the output of the sense amp.

4. The method of claim 3 wherein the data array is implemented as memory having a plurality of banks, with each applied address associated with one or more lines in one of the banks and not associated with lines in at least a portion of the plurality of banks, the method further comprising, between the time that an address is applied to the tag array and an output is provided from the sense amp, performing a memory operation in a bank in the portion of the plurality of banks.

5. The method of claim 1 wherein the at least one way comprises 2 ways.

6. The method of claim 5 wherein the at least one way consists of 4 ways.

7. The method of claim 1 wherein making a determination comprises for each way in the cache: reading a tag field from a location in the tag array and comparing the value in the tag field to a portion of the bits in the applied address.

8. The method of claim 7 additionally comprising controlling the charge on each of the plurality of lines in the data array to place the lines in a predetermined state before starting to alter the state of the line.

9. The method of claim 1 wherein each of the lines comprises a column line in the memory and altering the state of at least one line comprises asserting a word line in the memory.

10. A computer system having a cache, comprising:

a) a core having a memory address output with a plurality of bits;

b) a cache comprising:

i) a tag array having an output and an address input coupled to a first portion of the plurality of bits of the memory address output of the core, the tag array providing at its output information stored in the tag array in response to a value at the address input;

ii) a comparator having a first input coupled to the output of the tag array and a second input coupled to a second portion of the plurality of bits of the memory address output of the core and an output, the comparator providing an output at a first time in response to a memory address output by the core;

iii) a data array organized as a plurality of ways implemented in a semiconductor memory having a timing input, the semiconductor memory comprising:

A) an address input

B) a plurality of lines;

C) a plurality of memory cells connected to the lines to alter the charge on the lines selectively in response to the address input at a time indicated by the timing input;

D) a plurality of sense amps, with each line connectable to a sense amp, each sense amp having (I) an output indicating a value read from a line and (II) an enable input;

iii) a control circuit outputting a plurality of timing signals, with a first timing signal coupled to the timing input of the data array and a second timing signal connected to the enable input of the sense amp, wherein the second timing signal occurs after the first timing signal and before the first time.

11. The computer system of claim 10 wherein the first timing signal and the second timing signal are derived from clocks of the same frequency with different phases.

12. The computer system of claim 11 wherein the first timing signal and the second timing signal are derived from different phases of the same clock.

13. The computer system of claim 10 wherein the control circuit comprises a delay element having an input and an output, and the first timing signal is applied to the input of the delay element and the second timing signal is derived from the output of the delay element.

14. The computer system of claim 10 additionally comprising a charging circuitry having a plurality of drivers, each coupled to at least one line.

15. The computer system of claim 10 wherein each of the plurality of drivers has a control input to selectively disable the driver.

16. The computer system of claim 15 wherein the control circuit has outputs coupled to the plurality of drivers to disable at least one driver selectively in response to the address input coincident with the timing input.

17. The computer system of claim 10 additionally comprising a plurality of multiplexer circuits having a plurality of inputs and an output, each input coupled to one of the lines and the output coupled to one of the sense amps.

18. The computer system of claim 10 implemented as a semiconductor data processing chip.

19. A portable electronic device including the computer system of claim 18, the portable electronic device additionally comprising:

a) a memory separate from the semiconductor data processing chip; and

b) a battery connected to supply power to the semiconductor data processing chip and the memory.

20. The computer system of claim 10 wherein the control circuit generates the first timing signal and the second timing signal synchronous to a common clock.

21. The computer system of claim 10 wherein the control circuit generates the second timing signal a predetermined delay after the first timing signal.

22. A method of operating a cache in a computer system, the cache storing items associated with addresses in memory in the computer system, the cache having a tag array and a data array, the data array having a plurality of ways with information in the tag array indicating, for each address applied to the cache, in which, if any, way in the data array information associated with the applied address is stored, with the data array implemented as arrays of cells connected to lines and plurality of sense amps, with a sense amp being connectable to each of the word lines,

a) applying a first portion of the applied address to the tag array to address a location in each way of the tag array;

b) comparing a second portion of the applied address to information read from the addressed locations in each way of the tag array to produce at a first time, an indication of a match between the first input and one of the ways;

c) before the first time, altering the state of lines associated with the first portion of the applied address in each way of the data array, with the state of the lines based on information stored in the data array; and

d) after the first time, sensing the state of a line associated with the first portion of the applied address in the data array, with the sensed line selected in response to the output of the comparator.

23. The method of operating a cache in a computer system of claim 22 wherein each of the lines comprises a bit line in a semiconductor memory.

24. The method of operating a cache in a computer system of claim 23 wherein altering the state of lines comprises activating a cell connected to a word line in the semiconductor memory.

25. The method of operating a cache in a computer system of claim 22 additionally comprising placing the lines in a predetermined charge state.

26. The method of operating a cache in a computer system of claim 25 wherein altering the state of the lines comprises altering the charge on each line based on information stored in one memory cell.

27. The method of operating a cache in a computer system of claim 26 wherein each of the lines comprises a differential pair and altering the charge on the line comprises altering the charge difference between the lines.

28. The method of claim 22 wherein sensing the state of a line comprises enabling a sense amp selected based on the indication of a match.

29. The method of claim 22 wherein sensing the state of a line comprises activating a multiplexer based on the indication of a match to connect a selected line to a sense amp.